CLAIMS

1. A circuit comprising:

an input circuit for receiving an input signal, said input circuit including an input node, a first output node N1, and a path connecting said input and output nodes;

first means for applying a first current to said node N1 during a first mode of operation but not during a second mode; and

second means for applying a second current to said node N1 during both of said first and second modes.

2. The invention of Claim 1 wherein the value of said first current is determined such that the total current in said path is constant during said first and second modes.

3. The invention of Claim 1 wherein said circuit further includes third means for level shifting said input signal at said node N1 to a second output node N2.

4. The invention of Claim 3 wherein said first current is equal to a current drawn by said third means at said node N1 during said first mode.

5. The invention of Claim 3 wherein said first means includes a current switching circuit.

6. The invention of Claim 5 wherein said current switching circuit is configured to receive a first signal and in accordance therewith apply said first current to said node N1.

7. The invention of Claim 6 wherein said current switching circuit is also configured to receive a second signal and in accordance therewith apply said first current to said second node N2.

8. The invention of Claim 7 wherein said first signal is complementary to said second signal.

9. The invention of Claim 8 wherein said current switching circuit includes a differential pair of transistors Q12 and Q13.

10. The invention of Claim 9 wherein the emitters of said transistors Q12 and Q13 are connected in common to a first end of a first current source.

11. The invention of Claim 10 wherein a second end of said first current source is connected to a low voltage supply Vns.

12. The invention of Claim 11 wherein a collector of transistor Q12 is connected to said first node N1.

13. The invention of Claim 12 wherein a collector of transistor Q13 is connected to said second node N2.

14. The invention of Claim 13 wherein a base of transistor Q12 is connected to said first signal.

15. The invention of Claim 14 wherein a base of transistor Q13 is connected to said second signal.

16. The invention of Claim 1 wherein said second means includes a second current source.

17. The invention of Claim 16 wherein a first end of said second current source is coupled to said first node N1.

18. The invention of Claim 17 wherein a second end of said second current source is connected to a low voltage supply Vns.

19. The invention of Claim 3 wherein said third means includes a diode Q14.

20. The invention of Claim 19 wherein a cathode of said diode Q14 is connected to said first node N1.

21. The invention of Claim 20 wherein an anode of said diode Q14 is connected to said second node N2.

22. The invention of Claim 19 wherein said third means further includes a third current source having a first end coupled to said second node N2 for applying a bias current to said diode Q14.

23. The invention of Claim 22 wherein a second end of said third current source is coupled to a high voltage supply Vps.

24. The invention of Claim 22 wherein said first current is equal to said bias current.

25. The invention of Claim 22 wherein said second current is equal to said bias current.

26. The invention of Claim 1 wherein said first current is equal to said second current.

27. The invention of Claim 1 wherein said input circuit includes a transistor Q1.

28. The invention of Claim 27 wherein a base of said transistor Q1 is adapted to receive said input signal.

29. The invention of Claim 27 wherein an emitter of said transistor Q1 is connected to said first node N1.

30. The invention of Claim 27 wherein a collector of said transistor Q1 is connected to a high voltage supply Vps.

31. The invention of Claim 1 wherein said first mode is a track mode.

32. The invention of Claim 1 wherein said second mode is a hold mode.

33. A circuit comprising:

an input circuit for receiving an input signal, said input circuit including an input node, a first output node N1, and a path connecting said input and output nodes;

a level shifting circuit for level shifting said input signal at said node N1 to a second node N2;

a current switching circuit configured to receive a track signal and in accordance therewith apply a first current from a first current source to said node N1 during a track mode, and configured to receive a hold signal and in accordance therewith apply said first current to said node N2 during a hold mode; and

a second current source for applying a second current to said node N1 during both of said track and hold modes.

34. The invention of Claim 33 wherein the value of said first current is determined such that the total current in said path is constant during said track and hold modes.

35. The invention of Claim 33 wherein said first current is equal to a current

drawn by said level shifting circuit at said node N1 during said track mode.

36. The invention of Claim 33 wherein said current switching circuit includes a differential pair of transistors Q12 and Q13 having emitters connected in common to said first current source.

37. The invention of Claim 36 wherein a collector of transistor Q12 is connected to said node N1 and a collector of transistor Q13 is connected to said node N2.

38. The invention of Claim 37 wherein a base of transistor Q12 is connected to said track signal and a base of transistor Q13 is connected to said hold signal.

39. The invention of Claim 33 wherein said level shifting circuit includes a diode Q14, wherein a cathode of said diode Q14 is connected to said node N1 and an anode of said diode Q14 is connected to said second node N2.

40. The invention of Claim 39 wherein said level shifting circuit further includes a third current source for applying a bias current to said diode Q14.

41. The invention of Claim 33 wherein said input circuit includes a transistor Q1 having a base adapted to receive said input signal and an emitter connected to said node N1.

42. A track and hold circuit comprising:

an input circuit for conveying an input signal, wherein said input circuit comprises:

an input buffer circuit for receiving said input signal, said input buffer circuit including an input node, a first output node N1, and a path connecting said input and output nodes;

a level shifting circuit for level shifting said input signal at said node N1

to a second node N2;

a current switching circuit configured to receive a track signal and in accordance therewith apply a first current from a first current source to said node N1 during a track mode, and configured to receive a hold signal and in accordance therewith apply said first current to said node N2 during a hold mode; and

a second current source for applying a second current to said node N1 during both of said track and hold modes;

a capacitor circuit for storing a voltage representative of said input signal;

a differential amplifier circuit configured to receive said track signal and in accordance therewith generate a first control signal, and configured to receive said hold signal and in accordance therewith generate a second control signal; and

a switching circuit coupled between said input circuit and said capacitor circuit and configured to receive said first and second control signals and in accordance therewith close and open.

43. The invention of Claim 42 wherein said track and hold circuit further includes an output circuit coupled to the capacitor circuit and configured to receive a voltage appearing across the capacitor and in accordance therewith generate an output signal.

44. The invention of Claim 42 wherein said track and hold circuit further includes a clamping circuit coupled to said switching circuit and adapted to receive said second control signal and in accordance therewith clamp the voltage on the switching circuit to isolate the input signal from the voltage representative of the input signal stored on the capacitor circuit.

45. The invention of Claim 42 wherein the value of said first current is determined such that the total current in said path is constant during said track and hold modes.

46. The invention of Claim 42 wherein said first current is equal to a current drawn by said level shifting circuit at said node N1 during said track mode.

47. The invention of Claim 42 wherein said current switching circuit includes a differential pair of transistors Q12 and Q13 having emitters connected in common to said first current source.

48. The invention of Claim 47 wherein a collector of transistor Q12 is connected to said node N1 and a collector of transistor Q13 is connected to said node N2.

49. The invention of Claim 48 wherein a base of transistor Q12 is connected to said track signal and a base of transistor Q13 is connected to said hold signal.

50. The invention of Claim 42 wherein said level shifting circuit includes a diode Q14, wherein a cathode of said diode Q14 is connected to said node N1 and an anode of said diode Q14 is connected to said second node N2.

51. The invention of Claim 50 wherein said level shifting circuit further includes a third current source for applying a bias current to said diode Q14.

52. The invention of Claim 51 wherein said first current is equal to said bias current.

53. The invention of Claim 51 wherein said second current is equal to said bias current.

54. The invention of Claim 42 wherein said first current is equal to said second current.

55. The invention of Claim 42 wherein said input buffer circuit includes a

transistor Q1 having a base adapted to receive said input signal and an emitter connected to said node N1.

56. A method for reducing current transients in a track and hold circuit including the steps of:

receiving an input signal in an input circuit including an input node, an output node N1, and a path connecting said input and output nodes;

applying a first current to said node N1 during both a track mode and a hold mode; and

applying a second current to said node N1 during said track mode but not during said hold mode, such that the total current in said path remains constant during both track and hold modes.